TI-31754

Patent Amendment

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

<u>Listing of Claims</u>

- 1 (Currently Amended). Circuitry for processing images and video, comprising:
 - a random access memory;
- a motion estimation hardware accelerator coupled to said random access memory;
- a transform coding hardware accelera or coupled to said random access memory; and
- a processor eou ling coupled to said andware accelerators and to said random access memory for executing software instructions for processing images and video, wherein some of the instructions initiate functions performed by one or more of said hardware accelerators such that the one or more hardware accelerators retrieve data from the random access memory performat unction on the data, and return a result to the processor.
- 2 (Original). The circuitry of claim 1 and further comprising a pixel interpolation hardware accelerator coupled to said random access memory.
- 3 (Original). The circuitry of claim 2 \ herein said pixel interpolation hardware accelerator performs a half-pixel interpolation. inction.
- 4 (Original). The circuitry of claim 1 wherein said motion estimation hardware accelerator includes circuitry for calculating a mean absolute difference function.
- 5 (Original). The circuitry of claim 1 wherein said cansform coding hardware accelerator includes circuitry for calculating a direct cosine transform function.

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6 (Original). The circuitry of claim 5 wherein sai transform coding hardware are elerator includes circuitry for calculating an inverse rect cosine transform function.

7 (Currently Amended). A method of processi ; video information, comprising the steps of:

executing a compression task in a programmable processing device coupled to a random access memory;

upon encountering a motion estimation instruction, initiating execution of an at 5 ociated function in a motion estimation hardware accelerator coupled to said processing device and said random access in emory, such that the motion estimation hardware accelerator retrieves image data from the random access memory, performs a motion estimation function on the data, and returns a result to the processor; and

upon encountering a transform coding instruction initiating execution of an associated function in a transform coding hardware accelerator, said transform coding hardware accelerator coupled to said processing device and said random access the mory, such that the transform coding hardware accelerator retrieves image data from the random access memory, performs a transform coding function on the data, and returns a result to the processor.

8 (Currently Amended). The method of claim is step of initiating execution of an inssociated function in the motion estimation hardware accelerator includes the step of retrieving image data from a data portion of said random access memory into said motion estimation hardware accelerator.

9 (Currently Amended). The method of claim step of initiating execution of an issociated function in the transform coding hardwar accelerator includes the step of retrieving image data from a data portion of said rando access memory into said transform coding hardware accelerator.

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10 (Cui intly Amended). The method of claim 7 and furthe comprising the step of, upon associated fur tion in a pixel interpolation hardware accelerator, so pixel interpolation access memor such that the pixel interpolation hardware accelerator coupled to said processing devi and said random access memor such that the pixel interpolation hardware accelerator on the data, and returns a resu to the processor.

11 (Ori nal). The method of claim 10 wherein said step of in ating execution of an associated unction in a pixel interpolation hardware accelerator ucludes the step of performing a ulf-pixel interpolation function.

12 (Ori nal). The method of claim 7 wherein said step of init ting execution of an associated and an associated and an associated and an associated and a motion estimation hardware accelerator and a control of the step of

13 (Ori nal). The method of claim 7 wherein said step of init ting execution of an associated unction in a transform coding hardware accelerator is ludes the step of performing a rect cosine transform function.

14 (Ori nal). The method of claim 13 wherein said step of in ating execution of an associated unction in a transform coding hardware accelerator in ludes the step of performing at inverse direct cosine transform function.